Zynq Technical Reference Manual

This book constitutes the proceedings of the 19th International Conference on Cryptographic Hardware and Embedded Systems, CHES 2017, held in Taipei, Taiwan, in September 2017. The 33 full papers presented in this volume were carefully reviewed and selected from 130 submissions. The annual CHES conference highlights new results in the design and analysis of cryptographic hardware and soft- ware implementations. The workshop builds a valuable bridge between the research and cryptographic engineering communities and attracts participants from industry, academia, and government organizations.

This book presents the original concepts and modern techniques for specification, synthesis, optimisation and implementation of parallel logical control devices. It deals with essential problems of reconfigurable control systems like dependability, modularity and portability. Reconfigurable systems require a wider variety of design and verification options than the application-specific integrated circuits. The book presents a comprehensive selection of possible design techniques. The diversity of the modelling approaches covers Petri nets, state machines and activity diagrams. The preferences of the presented optimization and synthesis methods are not limited to increasing of the efficiency of resource use. One of the biggest advantages of the presented methods is the platform independence, the FPGA devices and single board computers are some of the examples of possible platforms. These issues and problems are illustrated with practical cases of

complete control systems. If you expect a new look at the reconfigurable systems designing process or need ideas for improving the quality of the project, this book is a good choice.g process or need ideas for improving the quality of the project, this book is a good choice.

Over the past decade, system-on-chip (SoC) designs have evolved to address the ever increasing complexity of applications, fueled by the era of digital convergence. Improvements in process technology have effectively shrunk board-level components so they can be integrated on a single chip. New on-chip communication architectures have been designed to support all inter-component communication in a SoC design. These communication architecture fabrics have a critical impact on the power consumption, performance, cost and design cycle time of modern SoC designs. As application complexity strains the communication backbone of SoC designs, academic and industrial R&D efforts and dollars are increasingly focused on communication architecture design. On-Chip Communication Architecures is a comprehensive reference on concepts, research and trends in on-chip communication architecture design. It will provide readers with a comprehensive survey, not available elsewhere, of all current standards for on-chip communication architectures. A definitive guide to on-chip communication architectures, explaining key concepts, surveying research efforts and predicting future trends Detailed analysis of all popular standards for on-chip communication architectures Comprehensive survey of all research on communication architectures, covering a wide range of topics relevant to this area, spanning the

past several years, and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures over the next several years

The two-volume set LNICST 209-210 constitutes the post-conference proceedings of the 11th EAI International Conference on Communications and Networking, ChinaCom 2016, held in Chongqing, China, in September 2016. The total of 107 contributions presented in these volumes are carefully reviewed and selected from 181 submissions. The book is organized in topical sections on MAC schemes, traffic algorithms and routing algorithms, security, coding schemes, relay systems, optical systems and networks, signal detection and estimation, energy harvesting systems, resource allocation schemes, network architecture and SDM, heterogeneous networks, IoT (Internet of Things), hardware design and implementation, mobility management, SDN and clouds, navigation, tracking and localization, future mobile networks.

This book constitutes the proceedings of the 33rd International Conference on Architecture of Computing Systems, ARCS 2020, held in Aachen, Germany, in May 2020. The 12 full papers in this volume were carefully reviewed and selected from 33 submissions. 6 workshop papers are also included. ARCS has always been a conference attracting leading-edge research outcomes in Computer Architecture and Operating Systems, including a wide spectrum of topics ranging from embedded and real-time systems all the way to large-scale and parallel systems. The selected papers focus on concepts and tools for incorporating self-adaptation*

*and self-organization mechanisms in high-performance computing systems. This includes upcoming approaches for runtime modifications at various abstraction levels, ranging from hardware changes to goal changes and their impact on architectures, technologies, and languages. *The conference was canceled due to the COVID-19 pandemic.*

This book contains extended and revised versions of the best papers presented at the 23rd IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2015, held in Daejeon, Korea, in October 2015. The 10 papers included in the book were carefully reviewed and selected from the 44 full papers presented at the conference. The papers cover a wide range of topics in VLSI technology and advanced research. They address the current trend toward increasing chip integration and technology process advancements bringing about new challenges both at the physical and system-design levels, as well as in the test of these systems.

This book constitutes the proceedings of the 32nd International Conference on Architecture of Computing Systems, ARCS 2019, held in Copenhagen, Denmark, in May 2019. The 24 full papers presented in this volume were carefully reviewed and selected from 40 submissions. ARCS has always been a conference attracting leading-edge research outcomes in Computer Architecture and Operating Systems, including a wide spectrum of topics ranging from embedded and real-time systems all the way to large-scale and parallel systems. The selected papers are organized in the following topical sections: Dependable systems; real-time systems; special

applications; architecture; memory hierarchy; FPGA; energy awareness; NoC/SoC. The chapter 'MEMPower: Data-Aware GPU Memory Power Model' is open access under a CC BY 4.0 license at link.springer.com.

The five-volume set LNCS 9786-9790 constitutes the refereed proceedingsof the 16th International Conference on Computational Science and ItsApplications, ICCSA 2016, held in Beijing, China, in July 2016. The 239 revised full papers and 14 short papers presented at 33 workshops were carefully reviewed and selected from 849 submissions. They are organized in five thematical tracks: computational methods, algorithms and scientific applications; high performance computing and networks; geometric modeling, graphics and visualization; advanced and emerging applications; and information systems and technologies.

Beitrag zur Integration und Analyse sicherheitstechnischer Maßnahmen bei der Entwicklung eines kompletten Rechners auf FPGA-Basis

Image Processing in Agriculture and Forestry

Embedded System Design

International Conference on Applications and Techniques in Cyber Security and Intelligence ATCI 2018

16th International Symposium, ARC 2020, Toledo, Spain, April 1–3, 2020, Proceedings

14th International Symposium, ARC 2018, Santorini, Greece, May 2-4, 2018, Proceedings

9th International Conference, NSS 2015, New York, NY, USA, November 3-5, 2015,

Proceedings
System on Chip Interconnect
Self Aware Security for Real Time Task Schedules in Reconfigurable Hardware Platforms
Doctoral Dissertation Colloquium 2014
Network and System Security
11th EAI international Conference, ChinaCom 2016 Chongqing, China, September 24-26, 2016, Proceedings, Part II
Information and Communication Technology for Intelligent Systems (ICTIS 2017) -

This four volume set LNCS 9528, 9529, 9530 and 9531 constitutes the refereed proceedings of the 15th International Conference on Algorithms and Architectures for Parallel Processing, ICA3PP 2015, held in Zhangjiajie, China, in November 2015. The 219 revised full papers presented together with 77 workshop papers in these four volumes were carefully reviewed and selected from 807 submissions (602 full papers and 205 workshop papers). The first volume comprises the following topics: parallel and distributed architectures; distributed and network-based computing and internet of things and cyber-physical-social computing. The second volume comprises topics such as big data and its applications and parallel and distributed algorithms.

The topics of the third volume are: applications of parallel and distributed computing and service dependability and security in distributed and parallel systems. The covered topics of the fourth volume are: software systems and programming models and performance modeling and evaluation.

This book describes a cross-domain architecture and design tools for networked complex systems where application subsystems of different criticality coexist and interact on networked multi-core chips. The architecture leverages multi-core platforms for a hierarchical system perspective of mixed-criticality applications. This system perspective is realized by virtualization to establish security, safety and real-time performance. The impact further includes a reduction of time-to-market, decreased development, deployment and maintenance cost, and the exploitation of the economies of scale through cross-domain components and tools. Describes an end-to-end architecture for hypervisor-level, chip-level, and cluster level. Offers a solution for different types of resources including processors, on-chip communication, off-chip communication, and I/O. Provides a cross-domain approach with

examples for wind-power, health-care, and avionics. Introduces hierarchical adaptation strategies for mixed-criticality systems Provides modular verification and certification methods for the seamless integration of mixed-criticality systems. Covers platform technologies, along with a methodology for the development process. Presents an experimental evaluation of technological results in cooperation with industrial partners. The information in this book will be extremely useful to industry leaders who design and manufacture products with distributed embedded systems in mixed-criticality use-cases. It will also benefit suppliers of embedded components or development tools used in this area. As an educational tool, this material can be used to teach students and working professionals in areas including embedded systems, computer networks, system architecture, dependability, real-time systems, and avionics, wind-power and health-care systems.

This book focuses on metaheuristic methods and its applications to real-world problems in Engineering. The first part describes some key metaheuristic methods, such as Bat Algorithms, Particle Swarm Optimization, Differential Evolution, and Particle

Collision Algorithms. Improved versions of these methods and strategies for parameter tuning are also presented, both of which are essential for the practical use of these important computational tools. The second part then applies metaheuristics to problems, mainly in Civil, Mechanical, Chemical, Electrical, and Nuclear Engineering. Other methods, such as the Flower Pollination Algorithm, Symbiotic Organisms Search, Cross-Entropy Algorithm, Artificial Bee Colonies, Population-Based Incremental Learning, Cuckoo Search, and Genetic Algorithms, are also presented. The book is rounded out by recently developed strategies, or hybrid improved versions of existing methods, such as the Lightning Optimization Algorithm, Differential Evolution with Particle Collisions, and Ant Colony Optimization with Dispersion – state-of-the-art approaches for the application of computational intelligence to engineering problems. The wide variety of methods and applications, as well as the original results to problems of practical engineering interest, represent the primary differentiation and distinctive quality of this book. Furthermore, it gathers contributions by authors from four countries – some of which are the original

proponents of the methods presented – and 18 research centers around the globe.

This book constitutes the proceedings of the 9th International Conference on Network and System Security, NSS 2015, held in New York City, NY, USA, in November 2015. The 23 full papers and 18 short papers presented were carefully reviewed and selected from 110 submissions. The papers are organized in topical sections on wireless security and privacy; smartphone security; systems security; applications security; security management; applied cryptography; cryptosystems; cryptographic mechanisms; security mechanisms; mobile and cloud security; applications and network security.

This book consists of twelve different contributions that reflect several aspects of OC research. Therefore, we introduced four major categories summarizing the contents of the contributions as well as describing the different aspects of OC research in general: (1) design and architectures, (2) trustworthiness, (3) self-learning, and (4) self-x properties.

This volume includes 74 papers presented at ICTIS 2017: Second International Conference on Information and Communication

Technology for Intelligent Systems. The conference was held on 25th and 26th March 2017, in Ahmedabad, India and organized jointly by the Associated Chambers of Commerce and Industry of India (ASSOCHAM) Gujarat Chapter, the G R Foundation, the Association of Computer Machinery, Ahmedabad Chapter and supported by the Computer Society of India Division IV – Communication and Division V – Education and Research. The papers featured mainly focus on information and communications technology (ICT) for computation, algorithms and data analytics. The fundamentals of various data analytics and algorithms discussed are useful to researchers in the field.

Embedded System Design: Modeling, Synthesis and Verification introduces a model-based approach to system level design. It presents modeling techniques for both computation and communication at different levels of abstraction, such as specification, transaction level and cycle-accurate level. It discusses synthesis methods for system level architectures, embedded software and hardware components. Using these methods, designers can develop applications with high level models, which are automatically translatable to low level implementations.

This book, furthermore, describes simulation-based and formal verification methods that are essential for achieving design confidence. The book concludes with an overview of existing tools along with a design case study outlining the practice of embedded system design. Specifically, this book addresses the following topics in detail: . System modeling at different abstraction levels . Model-based system design . Hardware/Software codesign . Software and Hardware component synthesis . System verification This book is for groups within the embedded system community: students in courses on embedded systems, embedded application developers, system designers and managers, CAD tool developers, design automation, and system engineering.

This book addresses a wide range of topics in areas of intelligent systems and artificial intelligence and their real-world applications. The 22 chapters have been selected from the 168 papers published in the proceedings of the SAI Intelligent Systems Conference 2016 (IntelliSys 2016), which received highly positive feedback in peer reviews. The IntelliSys 2016 conference was held in London on 21–22 September 2016. This

fascinating book offers readers state-of-the-art intelligent methods and techniques for solving real-world problems along with a vision of future research.

Exploring Zynq Mpsoc

13th International Symposium, ARC 2017, Delft, The Netherlands, April 3-7, 2017, Proceedings

Fundamentals, Advanced Features, and Applications in Industrial Electronics

Applications and Techniques in Cyber Security and Intelligence

Intelligent Systems and Applications

Using Vivado

Computational Science and Its Applications – ICCSA 2016

Schaltungs- und System-Design mit VHDL und C/C++

19th International Conference, Taipei, Taiwan, September 25-28, 2017, Proceedings

23rd IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2015, Daejeon, Korea, October 5-7, 2015, Revised Selected Papers

FPGA Based Accelerators for Financial Applications

Communications and Networking

21st International Conference, ICICS 2019, Beijing, China, December 15–17, 2019, Revised Selected Papers

A frequent market demand for functional safety managers reflected the grade of the importance the functional safety won in last few years. Analyzing the past two decades we could see that this science was reserved for aviation and process industry. Today, it is present in mostly industrial sectors. It did not lose its systematical and rigorous character despite significant modifications and changes. The capability of universal use becomes the manifest in generic concept of the world wide established safety standard IEC 61508. It derivates the instances for various branches as automotive, medicine, railway etc. In parallel to FPGA a similar progress path can be recognized - specialized applications at the beginning, then frequent use for testing purposes and prototyping, while today it is an integral part of daily life. As a design platform, FPGA provides very efficient and timing pragmatic development capabilities. But these aspects cannot be trivially transferred in a domain of the safety relevant applications. The presented

study focusses on this relation and provides a detailed analysis of the novel design flows of the leading FPGA manufacturers with the intention to evaluate whether the current FPGA structures are appropriate for the functional safety field. The primary scope is related to the implementation and evaluation of the On-Chip-Redundancy concept by implementing a SIL2 conform system The initial phase of this study was the development of complete computer architecture on the FPGA-based softcore 32-bit microcontroller. After successful system implementation, various internal and external safety measures that implicated a reduction of the common cause failures on an acceptable level, as well as an increase of the diagnostic coverage, have been integrated. In order to evaluate the safety of the system, the failure rate of each system component will be calculated using two different methods - gate equivalency and Xilinx reliability calculator. Validation of this concept is done by calculating the mean value of these two methods. In the context of the safety evaluation, we carried out an intense thermodynamic analysis in the form of a complex and reliable

simulation whose results significantly correlate with practical results.

The two-volume set, LNCS 11098 and LNCS 11099 constitutes the refereed proceedings of the 23nd European Symposium on Research in Computer Security, ESORICS 2018, held in Barcelona, Spain, in September 2018. The 56 revised full papers presented were carefully reviewed and selected from 283 submissions. The papers address issues such as software security, blockchain and machine learning, hardware security, attacks, malware and vulnerabilities, protocol security, privacy, CPS and IoT security, mobile security, database and web security, cloud security, applied crypto, multi-party computation, SDN security.

This book constitutes the refereed proceedings of the 21th International Conference on Information and Communications Security, ICICS 2019, held in Beijing, China, in December 2019. The 47 revised full papers were carefully selected from 199 submissions. The papers are organized in topics on malware analysis and detection, IoT and CPS security enterprise

network security, software security, system security, authentication, applied cryptograph internet security, machine learning security, machine learning privacy, Web security, steganography and steganalysis.

Reconfigurable Computing Systems Engineering: Virtualization of Computing Architecture describes the organization of reconfigurable computing system (RCS) architecture and discusses the pros and cons of different RCS architecture implementations. Providing a solid understanding of RCS technology and where it's most effective, this book: Details the architecture organization of RCS platforms for application-specific workloads Covers the process of the architectural synthesis of hardware components for system-on-chip (SoC) for the RCS Explores the virtualization of RCS architecture from the system and on-chip levels Presents methodologies for RCS architecture run-time integration according to mode of operation and rapid adaptation to changes of multi-parametric constraints Includes illustrative examples, case studies, homework problems, and references to important literature A

solutions manual is available with qualifying course adoption. Reconfigurable Computing Systems Engineering: Virtualization of Computing Architecture offers a complete road map to the synthesis of RCS architecture, exposing hardware design engineers, system architects, and students specializing in designing FPGA-based embedded systems to novel concepts in RCS architecture organization and virtualization.

The theme for the November 2017 conference was Striving for 100% Success Rate. Papers focus on the tools and techniques needed for maximizing the success rate in every aspect of the electronic device failure analysis process.

Im Rahmen dieser Arbeit wurden Fahrhinweise entwickelt, die den Fahrer dabei unterstützen sollen, seine Fahraufgabe möglichst energieeffizient zu meistern. Bei den Fahrhinweisen handelt es sich um ein Fahrerassistenzsystem. Die Fahrhinweise wurden implementiert und in einer Probandenstudie auf ihrer Wirkungsweise überprüft. - In this work, the author developed driver advices, that help the driver to perform his driving task in an efficient way. This advices are

classified as a driver assistance system. They have been implemented and their influence on the driver has been investigated during a case study.

This book constitutes the refereed proceedings of the 12th International Symposium on Applied Reconfigurable Computing, ARC 2016, held in Rio de Janeiro, Brazil, in March 2016. The 20 full papers presented in this volume were carefully reviewed and selected from 47 submissions. They are organized in topical headings named: video and image processing; fault-tolerant systems; tools and architectures; signal processing; and multicore systems. In addition, the book contains 3 invited papers and 8 poster papers on funded RD running and completed projects.

This book describes for readers a methodology for dynamic power estimation, using Transaction Level Modeling (TLM). The methodology exploits the existing tools for RTL simulation, design synthesis and SystemC prototyping to provide fast and accurate power estimation using Transaction Level Power Modeling (TLPM). Readers will benefit from this innovative way

of evaluating power on a high level of abstraction, at an early stage of the product life cycle, decreasing the number of the expensive design iterations.

Safer and More Efficient Future Driving
On-Chip Communication Architectures
Information and Communications Security
Organic Computing
Extended and Selected Results from the SAI Intelligent Systems Conference (IntelliSys) 2016
FPGA-BASED Hardware Accelerators
16th International Conference, Beijing, China, July 4-7, 2016, Proceedings
Applied Reconfigurable Computing
Functional Verification of Dynamically Reconfigurable FPGA-based Systems
VLSI-SoC: Design for Reliability, Security, and Low Power
Algorithms and Architectures for Parallel Processing
32nd International Conference, Copenhagen, Denmark, May 20–23, 2019, Proceedings

Architecture of Computing Systems – ARCS 2019

This book constitutes the proceedings of the 14th International Conference on Applied Reconfigurable Computing, ARC 2018, held in Santorini, Greece, in May 2018. The 29 full papers and 22 short presented in this volume were carefully reviewed and selected from 78 submissions. In addition, the volume contains 9 contributions from research projects. The papers were organized in topical sections named: machine learning and neural networks; FPGA-based design and CGRA optimizations; applications and surveys; fault-tolerance, security and communication architectures; reconfigurable and adaptive architectures; design methods and fast prototyping; FPGA-based design and applications; and special session: research projects.

This book helps readers to implement their designs on Xilinx® FPGAs. The authors demonstrate how to get the greatest impact from using the Vivado® Design Suite, which delivers a SoC-strength, IP-centric and system-centric, next generation development environment that has been built from the ground up to address the productivity bottlenecks in system-level integration and implementation. This book is a hands-on guide for both users who are new to FPGA designs, as well as those currently using the legacy Xilinx tool set (ISE) but are now moving to Vivado. Throughout the presentation, the authors focus on key concepts, major mechanisms for design entry, and methods to realize the most efficient implementation of the target design, with the least number of iterations. This book suggests and describes a number of fast parallel circuits for data/vector

processing using FPGA-based hardware accelerators. Three primary areas are covered: searching, sorting, and counting in combinational and iterative networks. These include the application of traditional structures that rely on comparators/swappers as well as alternative networks with a variety of core elements such as adders, logical gates, and look-up tables. The iterative technique discussed in the book enables the sequential reuse of relatively large combinational blocks that execute many parallel operations with small propagation delays. For each type of network discussed, the main focus is on the step-by-step development of the architectures proposed from initial concepts to synthesizable hardware description language specifications. Each type of network is taken through several stages, including modeling the desired functionality in software, the retrieval and automatic conversion of key functions, leading to specifications for optimized hardware modules. The resulting specifications are then synthesized, implemented, and tested in FPGAs using commercial design environments and prototyping boards. The methods proposed can be used in a range of data processing applications, including traditional sorting, the extraction of maximum and minimum subsets from large data sets, communication-time data processing, finding frequently occurring items in a set, and Hamming weight/distance counters/comparators. The book is intended to be a valuable support material for university and industrial engineering courses that involve FPGA-based circuit and system design.

The book highlights innovative ideas, cutting-edge findings, and novel

techniques, methods and applications touching on all aspects of technology and intelligence in smart city management and services. Above all, it explores developments and applications that are of practical use and value for Cyber Intelligence-related methods, which are frequently used in the context of city management and services.

Für einen erfolgreichen Hardware Entwurf sind nicht nur VHDL-Kenntnisse wichtig, sondern auch Kenntnisse der FPGA-Schaltungstechnik und der Design Tools. Das vorliegende Buch stellt die Zusammenhänge zwischen diesen wichtigen Themen dar und bietet eine zielgerichtete Einführung in den Entwurf von digitalen Schaltungen und Systemen mit FPGAs. Beginnend mit den Grundlagen von VHDL sowie der CMOS- und FPGA-Technologie, werden anschließend der synthesegerechte Entwurf mit VHDL und die synchrone Schaltungstechnik auf dem FPGA behandelt. Darüber hinaus werden auch die wesentlichen Entwurfswerkzeuge, wie Logiksynthese oder die statische Timing-Analyse, erläutert. Abgerundet wird das Buch mit einem Kapitel über High-Level Synthese, welche eine Umsetzung von C/C++-Code in eine VHDL-Implementierung ermöglicht. Der Leser erhält anhand vieler Code-Beispiele einen praxisorientierten Zugang zum Hardware-Entwurf mit FPGAs. Zielgerichtete Einführung in den digitalen Schaltungsentwurf Alle notwendigen Kenntnisse für den rechnergestützten Hardwareentwurf Frank Kesel studierte Elektrotechnik an der Universität Karlsruhe und promovierte an der Universität Hannover. Er war zehn Jahre in der Industrie im digitalen ASIC-Design tätig. Er ist seit 1999

Professor an der Hochschule Pforzheim mit dem Spezialgebiet FPGA-Design.
The main topics of this book include advanced control, cognitive data processing, high performance computing, functional safety, and comprehensive validation. These topics are seen as technological bricks to drive forward automated driving. The current state of the art of automated vehicle research, development and innovation is given. The book also addresses industry-driven roadmaps for major new technology advances as well as collaborative European initiatives supporting the evolvement of automated driving. Various examples highlight the state of development of automated driving as well as the way forward. The book will be of interest to academics and researchers within engineering, graduate students, automotive engineers at OEMs and suppliers, ICT and software engineers, managers, and other decision-makers.
Field Programmable Gate Arrays (FPGAs) are currently recognized as the most suitable platform for the implementation of complex digital systems targeting an increasing number of industrial electronics applications. They cover a huge variety of application areas, such as: aerospace, food industry, art, industrial automation, automotive, biomedicine, process control, military, logistics, power electronics, chemistry, sensor networks, robotics, ultrasound, security, and artificial vision. This book first presents the basic architectures of the devices to familiarize the reader with the fundamentals of FPGAs before identifying and discussing new resources that extend the ability of the devices to solve problems in new application domains. Design methodologies are discussed and application

examples are included for some of these domains, e.g., mechatronics, robotics, and power systems.

This book constitutes the proceedings of the 16th International Symposium on Applied Reconfigurable Computing, ARC 2020, held in Toledo, Spain, in April 2020. The 18 full papers and 11 poster presentations presented in this volume were carefully reviewed and selected from 40 submissions. The papers are organized in the following topical sections: design methods & tools; design space exploration & estimation techniques; high-level synthesis; architectures; applications.

With Pynq and Machine Learning Applications

Modeling, Synthesis and Verification

Transaction-Level Power Modeling

33rd International Conference, Aachen, Germany, May 25-28, 2020, Proceedings

Computational Intelligence, Optimization and Inverse Problems with Applications in Engineering

23rd European Symposium on Research in Computer Security, ESORICS 2018, Barcelona, Spain, September 3-7, 2018, Proceedings, Part I

Architecture of Computing Systems – ARCS 2020

Virtualization of Computing Architecture

Adaptive Fahrhinweise für ein längsdynamisches Fahrerassistenzsystem zur Steigerung der Energieeffizienz

Applied Reconfigurable Computing. Architectures, Tools, and Applications

Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All

Programmable Soc
Designing with Xilinx® FPGAs
Distributed Real-Time Architecture for Mixed-Criticality Systems

This book is about the Zynq-7000 All Programmable System on Chip, the family of devices from Xilinx that combines an application-grade ARM Cortex-A9 processor with traditional FPGA logic fabric. Catering for both new and experienced readers, it covers fundamental issues in an accessible way, starting with a clear overview of the device architecture, and an introduction to the design tools and processes for developing a Zynq SoC. Later chapters progress to more advanced topics such as embedded systems development, IP block design and operating systems. Maintaining a 'real-world' perspective, the book also compares Zynq with other device alternatives, and considers end-user applications. The Zynq Book is accompanied by a set of practical tutorials hosted on a companion website. These tutorials will guide the reader through first steps with Zynq, following on to a complete, audio-based embedded systems design.

This book constitutes the refereed proceedings of the 13th International Symposium on Applied Reconfigurable Computing, ARC 2017, held in Delft, The Netherlands, in April 2017. The 17 full papers and 11 short papers presented in this volume were carefully reviewed and selected from 49 submissions. They are organized in topical sections on adaptive architectures, embedded computing and security, simulation and synthesis, design space exploration, fault tolerance, FGPA-based designs, neural neworks, and languages and estimation techniques.

This book is a printed edition of the Special Issue "Image Processing in Agriculture and Forestry" that was published in J. Imaging

This book covers the latest approaches and results from reconfigurable computing architectures employed in the finance domain. So-called field-programmable gate arrays (FPGAs) have already shown to outperform standard CPU- and GPU-based computing architectures by far, saving up to 99% of energy depending on the compute tasks. Renowned authors from financial mathematics, computer architecture and finance business introduce the readers into today's challenges in finance IT, illustrate the most advanced approaches and use cases and present currently known methodologies for integrating FPGAs in finance systems together with latest results. The complete algorithm-to-hardware flow is covered holistically, so this book serves as a hands-on guide for IT managers, researchers and quants/programmers who think about integrating FPGAs into their current IT systems.

This book analyzes the challenges in verifying Dynamically Reconfigurable Systems (DRS) with respect to the user design and the physical implementation of such systems. The authors describe the use of a simulation-only layer to emulate the behavior of target FPGAs and accurately model the characteristic features of reconfiguration. Readers are enabled with this simulation-only layer to maintain verification productivity by abstracting away the physical details of the FPGA fabric. Two implementations of the simulation-only layer are included: Extended Re Channel is a System C library that can be used to check DRS designs at a high level; ReSim is a library to support RTL simulation of a DRS reconfiguring both its logic and

state. Through a number of case studies, the authors demonstrate how their approach integrates seamlessly with existing, mainstream DRS design flows and with well-established verification methodologies such as top-down modeling and coverage-driven verification.

This book introduces the Zynq MPSoC (Multi-Processor System-on-Chip), an embedded device from Xilinx. The Zynq MPSoC combines a sophisticated processing system that includes ARM Cortex-A53 applications and ARM Cortex-R5 real-time processors, with FPGA programmable logic. As well as guiding the reader through the architecture of the device, design tools and methods are also covered in detail: both the conventional hardware/software co-design approach, and the newer software-defined methodology using Xilinx's SDx development environment. Featured aspects of Zynq MPSoC design include hardware and software development, multiprocessing, safety, security and platform management, and system booting. There are also special features on PYNQ, the Python-based framework for Zynq devices, and machine learning applications. This book should serve as a useful guide for those working with Zynq MPSoC, and equally as a reference for technical managers wishing to gain familiarity with the device and its associated design methodologies.

Cryptographic Hardware and Embedded Systems – CHES 2017

ISTFA 2017: Proceedings from the 43rd International Symposium for Testing and Failure Analysis

FPGA Hardware-Entwurf

The Zynq Book

Automated Driving
15th International Conference, ICA3PP 2015, Zhangjiajie, China, November 18-20, 2015, Proceedings
Computer Security
12th International Symposium, ARC 2016 Mangaratiba, RJ, Brazil, March 22–24, 2016 Proceedings
ICCWS 2017 12th International Conference on Cyber Warfare and Security
FPGAs
Design of Reconfigurable Logic Controllers
Reconfigurable Computing Systems Engineering